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PATENT ABSTRACTS OF JAPAN

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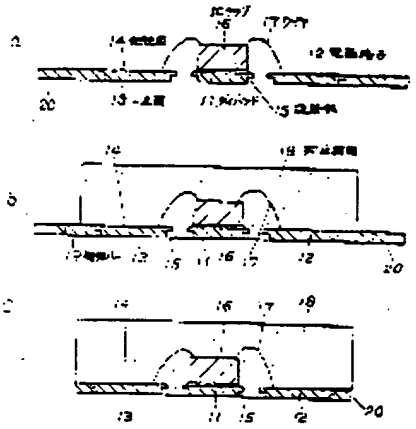
TAKASE YOSHIHISA

(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE



(57)Abstract:

PURPOSE: To make an electrode terminal not to come off due to external force and thermal strain by providing the end surface of a lead frame substrate with a stair part having more than one step and performing molding with sealing resin in a shape of covering the stair part.

CONSTITUTION: An IC chip 16 is mounted on the other main surface 14 of a die pad 11, and a pad of the IC chip and the other main surface 14 of an electrode terminal 12 are bonded with a wire 17 so as to be continuously molded with sealing resin 18 on the almost level with one main surface 13 by a transfer method so that the electrode terminal and the main surface 13 of the die pad 11 may be exposed. At this time, a stair part 15 provided on a lead frame 20 is also covered with sealing resin 18. Thereby, a reinforcing bar 19 exposed to an end surface of sealing resin 18 is also of the same projection type so as to have very strong structure against coming-off even to external force.

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⑲日本国特許庁（JP）　⑪特許出願公開

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審査請求　未請求　発明の数 1　（全4頁）

⑤4発明の名称　半導体集積回路装置

⑳特　願　昭62－263435
㉒出　願　昭62(1987)10月19日

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明　細　書

1、発明の名称

半導体集積回路装置

2、特許請求の範囲

複数の電極端子を有するリードフレームの一主面の面積が、他の主面より狭く、このリードフレームの断面形状は少なくとも1段以上の段差を持つ段差部を有するものであり、半導体集積回路は他の主面にマウントされ、少なくとも電極端子の一主面を露出した形で一主面と略ぼ平坦に封止樹脂が成形されている半導体集積回路装置。

3、発明の詳細な説明

産業上の利用分野

本発明は半導体集積回路をパッケージした半導体集積回路装置に関するものである。

従来の技術

ポータブルな情報ファイルとしてのICカードはカードの一部にメモリ，マイクロプロセッサを[illegible]する演算機能を持っているが、ISO規格によりカード厚みは最大0.84ミリとされており、当然半導体集積回路装置は更に薄くしかも厚み精度が強く要求される。

当初半導体集積回路装置の基板はガラスエポキシを基体とする両面基板が主流であったが、ガラスエポキシ基板ではICカード用半導体集積回路装置に要求する厚み精度を十分に満足させるものではなかった。

そこでガラスエポキシ基板の代りに厚み精度がよく半導体集積回路装置の総厚の厚み精度も向上させられるリードフレームを基板とするICカード用半導体集積回路装置が提案された。このICカード用半導体集積回路装置の構造を第4図に示し説明する。

複数本の電極端子1とダイパッド2を有するリードフレーム6の上記ダイパッド2にICチップ3がマウントされ、上記ICチップ3のパッド

5を露出した形で、しかも上記一主面5とほぼ平坦に封止樹脂6がトランスファ成形法により成形された構造となっている。

ところが上記電極端子1の上記一主面5は外部に露出し、上記電極端子1の薄い側面を含む片面しか上記封止樹脂6を接触していない。通常トランスファ成形法で成形する上記封止樹脂6中には成形金型との離形性をよくするために、離形剤が入れられていることから、当然上記電極端子1と上記封止樹脂6との密着性はよいものではない。この問題点を解決する方法として、上記封止樹脂6と接触する他の主面7を粗面化したり、上記電極端子1の一主面5の面積を他の主面7の面積より狭くして（エッジにテーパをつけ台形形状とする）密着性の向上を図っている。

発明が解決しようとする問題点

このような半導体集積回路装置に用いるリードフレーム8の厚味は、半導体集積回路装置に総厚の制限があることから0.15ミリ以下が通常用いられる。ところが封止樹脂6とリードフレーム8の他の主面7との密着性を強化するために、リードフレーム8の断面をテーパ加工し、わずかに封止樹脂6でリードフレーム8を覆う形としているが、リードフレーム8の厚味が0.15ミリと非常に薄いため、封止樹脂6でリードフレーム8の断面を一回覆う形とした場合でもせいぜい厚味分の0.15ミリ程度しか覆うことができず、端面にテーパをつけても封止樹脂6に対するリードフレーム8の密着強度を著しく向上させることはできなかった。また前にも述べたが封止樹脂6には離形剤が入っているため、リードフレーム8との密着性が悪く、例えば熱衝撃試験を行った時に発生する熱的ひずみによりリードフレーム8が剥れる可能性も生じてくる。更にトランスファ成形後リードフレーム8の補強バーを封止樹脂6の端面に沿ってほぼ平坦に金型にて切断して個片の半導体集積回路装置にするわけであるが、補強バーの切断面は金型で切断する際、わずかなバリが発生することと、完全に封止樹脂6の端面と平坦にすることは不可能で、わずかに切断面が突き出る形となる。この状態でカード化しカードの携帯中あるいは使用中に何らかの異物が切断面にできたバリ、あるいは電極端子自体にひっかかり電極端子をはがしてしまう可能性がある。このように電極端子がはがれたり、変形するとICカードとしての機能が全く失なわれることになる。

本発明は上記問題点を鑑み、外的な力、熱ひずみ等に対しても電極端子がはがれて使用不能にならないようなリードフレームの構造を提供するものである。

問題点を解決するための手段

そして上記問題点を解決する本発明の技術的手段は、リードフレームの一主面の面積を他の主面より狭くし断面形状を凸型として一主面とほぼ平坦に封止樹脂を成形し、リードフレームの端面を所定の距離、厚さでほぼ全辺にわたって封止樹脂で覆うように構成したものである。

作用

この構成により電極端子の接続金辺が封止樹脂からの力が加わらず、また熱衝撃試験等による熱ひずみに対しても電極端子が剥れることがないため信頼性の高い半導体集積回路装置を作ることが可能となる。

実施例

以下本発明の一実施例について図面を用いながら説明する。第2図a，bは本発明に用いたリードフレームの構造を示す。第2図aは上面図、第2図bはA－A'をみた断面図である。ダイパッド11、複数本の電極端子12で構成されており、上記ダイパッド11及び上記電極端子12の外部に露出する一主面13の面積は他の主面14より狭く、少なくとも封止樹脂で覆われる部分のリードフレーム20の断面は凸型の段差部15が設けられている。ちなみにリードフレーム20の厚味が0.15ミリの場合上記段差部15のTは0.05ミリ、Dは0.1ミリとした。上記段差部15の断面形状は段差が1段のみならず複数段形成されていてもかまわない。以上はダイパッド11が複数本

る構造のリードフレームである。このリードフレーム２０の作製方法は一実施例として、まずプレス機でストレートにパンチングした後続いて別の金型を用い同じくプレス機により リードフレーム２０の端面のみをプレスし所定の量だけ段差部15を作った。他の方法としてエッチングによる方法でも同様の段差部１５を作ることは可能である。以上の説明はＩＣチップを搭載するダイパッド11を有するリードフレーム２０であるが、ダイパッド１１の無い電極端子１２のみのリードフレームでもかまわない。

以上述べた段付きリードフレーム２０を用いた半導体集積回路装置の製造プロセスを第３図ａ～ｃに示す。これは第２図のＡ－Ａ'の断面を表わすものである。ダイパッド１１の他の主面１４にＩＣチップ１６をマウントし、上記ＩＣチップ16のパッド（図示せず）と上記電極端子１２の他の主面１４をワイヤ１７で接続し（第３図ｂ）、続いてトランスファ成形法にて上記電極端子１２、及びダイパッド１１の一主面１３を露出させるごとく、上記一主面１３とほぼ平坦に封止樹脂１８で成形する（第３図ｂ）。この時リードフレーム２０に設けられた段差部１５も上記封止樹脂１８で覆われる形となる。更に金型を用いて上記封止樹脂１８の端面に沿って補強バー１９を切断して個片の半導体集積回路装置とする（第３図ｃ）。以上のべた半導体集積回路装置の電極端子部の拡大図を第１図に示す。この第１図によれば電極端子１２の一主面と封止樹脂１８はほぼ平坦に成形されており、封止樹脂１８に埋設した電極端子12の一部は、露出している一主面より広がっている構造となっている。このことは、電極端子１２の端面に形成されている段差部１５を完全に封止樹脂１８が覆っていることになり、封止樹脂１８の端面に露出している補強バー１９と同様の凸型であることから外的な力に対しても非常に剥れに強い構造となっている。

以上述べてきた実施例の中でＩＣチップ１６のパッドと電極端子１２の接続にワイヤ１１を用いているが、ワイヤーボンディング法に限定するものではなく、バンプを利用したフリップチップボンディング方式でもかまわない。また同時にリードフレーム２０の他の主面側をニッチング、サンドブラストメッキ法等で粗面化処理が施こされていても良い。更にダイパッド１１が無くＩＣチップ１６が電極端子１２にかかるようなリードフレーム２０を用いる場合はＩＣチップ１６をマウントするダイボンド樹脂は絶縁性であることはいうまでもない。

発明の効果

本発明の半導体集積回路装置はリードフレーム基板の端面に１段以上の段差部を設け、段差部を覆う形で封止樹脂にて成形しているため、外的な力にも電極端子は剥れにくく、熱衝撃試験等の熱ひずみに対しても、電極端子ははがれないことから、信頼性の高いものを得ることが可能となる。

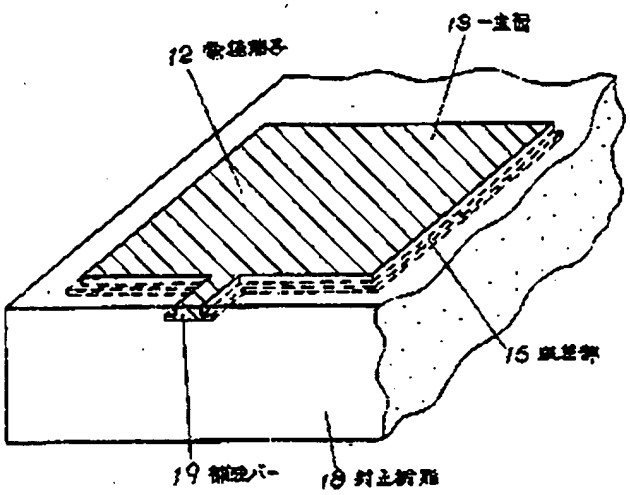
4、図面の簡単な説明

第１図は本発明の半導体集積回路装置の一実施例における電極端子部の拡大斜視図、第２図は上面図と断面図、第３図ａ～ｃは本発明の半導体集積回路装置の製造フローを示す断面図、第４図は従来のリードフレームを用いた半導体集積回路装置の構造を示す断面図である。

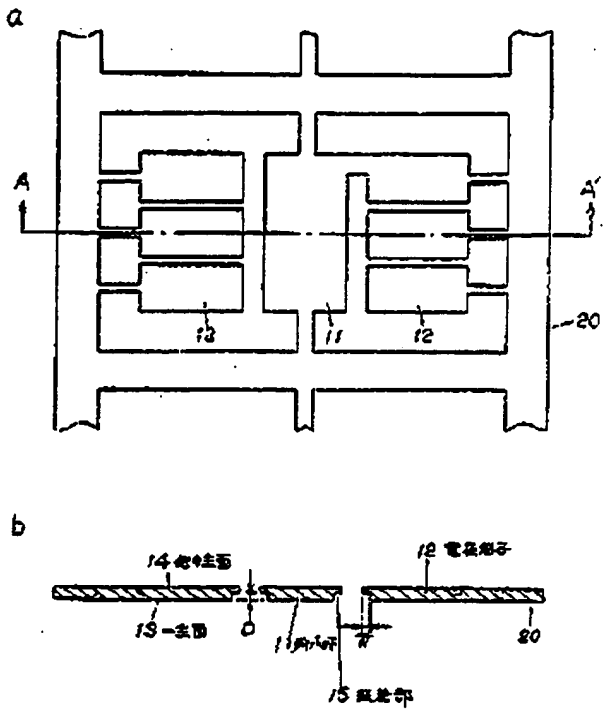
１２……電極端子、１３……一主面、１４……他の主面、１５……段差部、１６……ＩＣチップ、１７……ワイヤ、１８……封止樹脂、１９……補強バー、２０……リードフレーム。

代理人の氏名　弁理士　中　尾　敏　男　ほか１名

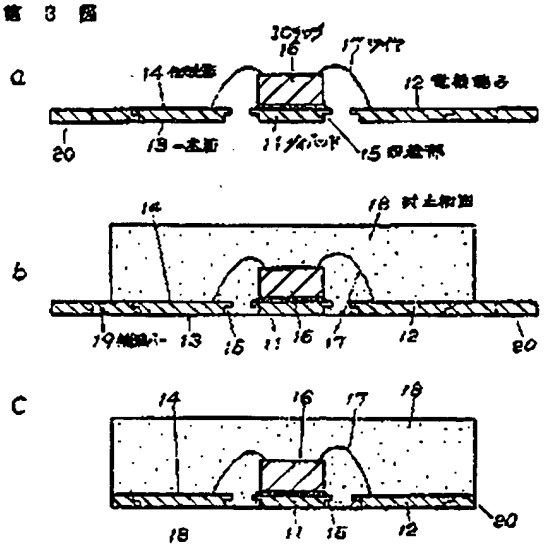
第 1 図



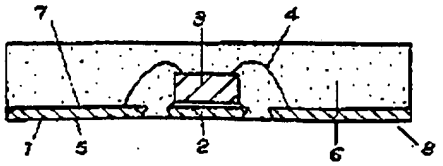
第 2 図



第 3 図



第 4 図



(19) JAPANESE PATENT OFFICE (JP)

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(43) Disclosure Date: 24 April 1989

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Number of Inventions: 1 (Total of 4 pages)

(54) Title of the Invention: Semiconductor Integrated Circuit Device

(21) Application No.: 62[1987]-263,435

(22) Application Date: 19 October 1987

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SPECIFICATION

1. Title of the Invention

Semiconductor Integrated Circuit Device

2. Claim

A semiconductor integrated circuit device in which the area of the main surface of the lead frame, which has several electrode terminals, is narrower than the other main surface, the cross-sectional shape of the lead frame has stair components having at least one or more steps, the semiconductor integrated circuit is mounted on the other main surface, and a sealing resin that is essentially even with the main surface is formed in a shape in which at least the main surfaces of the electrode terminals are exposed.

3. Detailed Description of the Invention

Field of Industrial Use

This invention relates to a semiconductor integrated surface device in which the semi-conductor integrated circuit is packaged.

Prior Art

A semiconductor integrated circuit device having a memory and a microprocessor is embedded in a part of an IC card, which serves as a portable information file. The card has the operational functions of reading and deleting. However, in accordance with ISO standards, the maximum thickness of the cards is 0.84 mm. Naturally, there is a demand for the semiconductor integrated circuits to be thinner, for greater precision of thickness and for greater strength.

Initially, the main trend is for the board of a semiconductor integrated circuit device to be a two-surface board having glass epoxy as the base substance. However, with a glass epoxy base substance, the precision of thickness required of semiconductor integrated circuit devices for IC cards could not be sufficiently satisfied.

Accordingly, a semiconductor integrated circuit device for IC cards was proposed in which a lead frame of which the precision of thickness was good and of which the thickness precision of the total thickness of the semiconductor integrated circuit device was improved was used as the board in place of a glass epoxy board. Figure 4 shows and illustrates the structure of this semiconductor integrated circuit device for IC cards.

The IC chip 3 is mounted on the die pad 2 of the lead frame 8, which has several electrode terminals 1 and the aforementioned die pad 2, the pad (not shown in the figure) of the aforementioned IC chip 3 and the aforementioned electrode terminals 1 are connected by the wires 4 and a structure is formed in a configuration in which at least the main surfaces 5 of the aforementioned electrode terminals 1 are exposed and in which the sealing resin 6 is formed by transfer molding essentially even with the aforementioned main surfaces 5.

However, the main surfaces 5 of the aforementioned electrode terminals 1 are exposed to the outside and only one surface, including the thin side faces of the aforementioned electrode terminals, is in contact with the aforementioned sealing resin 6. Because a release agent is usually introduced into the aforementioned sealing resin 6, which is formed by the transfer molding method,

in order to improve release from the mold, there is naturally poor adhesion between the aforementioned electrode terminals 1 and the aforementioned sealing resin 6. A method for solving this problem is to coarsen the other main surface 7 that is in contact with the aforementioned sealing resin 6 and make the area of main surface 5 of the aforementioned electrode terminals 1 narrower than the area of the other main surface 7 (by tapering the edge to give a trapezoid shape) in order to improve adhesion.

Problems the Invention Is Intended to Solve

Because the thickness of the lead frame 8 used in semiconductor integrated circuit devices is limited in this way by the total thickness of the semiconductor integrated circuit device, it is ordinarily 0.15 mm or less. However, in order to strengthen the adhesion between the sealing resin 6 and the other main surface 7 of the lead frame 8, the cross section of the lead frame 8 is tapered to a shape in which the lead frame 8 is very slightly covered by the sealing resin 6. Because the thickness of the lead frame 8 of 0.15 mm is extremely thin, even when there is a configuration in which the tip surface of the lead frame is partially covered, it can at most be covered only on an order of thickness of 0.15 mm, and, even when the tip surface is tapered, the adhesive strength of the lead frame 8 to the sealing resin 6 cannot be markedly improved. Further, as discussed previously, because a release agent is introduced into the sealing resin 6, there is poor adhesion to the lead frame 8. For example, there is the possibility that the lead frame will peel due to the thermal strain that occurs when thermal impact tests are performed. Moreover, after transfer molding, the

reinforcing bar of the lead frame 8 is cut in the mold so that it is essentially even along the tip surface of the sealing resin 6 to make a semiconductor integrated circuit device with individual sides. However, when the cut surface of the reinforcing bar is cut in the mold, very slight variations occur and it is not possible to make it completely even with the tip end of the sealing resin 6, for which reason the cut surface assumes a configuration in which it protrudes very slightly. In this state, there is the possibility that the electrode terminals will be peeled off as a result of being caught up in various structures formed by foreign objects in the cut surface during cutting of the card or during transport or use of the card or by peeling of the electrode terminal itself. When the electrode terminals are peeled off or deformed in this way, the function as an IC card is completely lost.

In view of the aforementioned problems, this invention provides a structure of a lead frame such that the electrode terminals are not peeled off and become useless, even in the presence of external force and thermal strain.

Means for Solving the Problems

The technological means whereby the aforementioned problems are solved is a structure such that the area of one main surface of the lead frame is made narrower than the other main surface, the cross-sectional shape involves a projection, the sealing resin is formed essentially even with one main surface and the end surface of the lead frame is covered by the sealing resin along almost the entire edge at a specified distance and thickness.

Action

Because almost the entire edges of the electrode terminals are covered by sealing resin due to this structure, no external force that peels the electrode terminals arises and the electrode terminals are not peeled off even in the presence of thermal strain due to impact tests, for which reasons a semiconductor integrated circuit device of high reliability can be made.

Examples

We shall now describe an example of this invention making use of the figures. Figures 2a and b show the structure of the lead frame that is used in this invention. Figure 2a is an upper surface view and Figure 2b is a cross-sectional view seen through A—A'. It is comprised of the die pad 11 and the multiple electrode terminals 12. The area of the one main surface 13 that is exposed on the outer side of the aforementioned die pad 11 and of the aforementioned electrode terminals 12 is narrower than that of the other main surface 14 and the protruding stair components 15 are established in the cross section of at least the part of the lead frame 20 that is covered by the sealing resin. In this connection, when the thickness of lead frame 20 is 0.15 mm, W [the width] of the aforementioned stair components 15 is set to 0.5 mm and D [the depth] is set to 0.1 mm. The cross-sectional shape of the aforementioned component may be not only a stair of one step but may also be formed as several steps. What is described above is a lead frame of a structure in which the die pad 11 is connected to at least one of the several electrode terminals 12. The following is an example of the method of manufacture of this lead frame 20. First, it is pressed flat with a pressing machine, after which only the end surface of the lead

frame 20 is similarly pressed by a pressing machine using a separate mold, with the stair components 15 being made in a specified amount. Similar stair components 15 can also be made by the etching method as another method. What is described above is a lead frame 20 having the die pad 11 for mounting the IC chip. However, it may also be a lead frame consisting only of the electrode terminals 12 without the die pad 11.

Figures 3a through c show the process of manufacture of a semiconductor integrated circuit device in which the stepped lead frame 20 as described above is used. They show the cross section through A – A' in Figure 2. The IC chip 16 is mounted on the other main surface 14 of the die pad 11. The pad (not shown in the figure) of the aforementioned IC chip 16 and the other main surface 14 of the aforementioned electrode terminals 12 are connected by the wires 17 (Figure 3a). Next, as the aforementioned electrode terminals 12 and the other main surface of the die pad 11 are exposed by the transfer molding method, the structure is formed with the sealing resin 18 essentially even with the aforementioned main surface 13 (Figure 3b). At this time, the stair components 15 that are established in the lead frame 20 assume a configuration in which they are also covered by the sealing resin 18. Further, the reinforcing bar 19 is cut along the end surface of the aforementioned sealing resin 18 using a mold, and an individual semiconductor integrated circuit device is formed (Figure 3c). Figure 1 shows an enlarged view of the electrode terminal components of the semiconductor integrated circuit device described above. As indicated in Figure 1, they are constructed so that one main surface of the electrode terminals 12 is

formed essentially even with the sealing resin 18 and that the portion of the electrode terminals that is embedded in the sealing resin 18 is wider than the one main surface that is exposed. This results in the sealing resin 18 completely covering the stair components 15 that are formed on the tip surface of the electrode terminals 12. Because the reinforcing bar that is exposed on the tip surface of the reinforcing resin 18 is of a similar protruding shape, a structure is formed that is extremely strong even in the presence of external force.

In the example described above, the wires 17 are used for connection of the pad of the IC chip 16 and the electrode terminals 12. However, this is not limited to the wire bonding method and the flip-chip bonding method using a bump may also be used. At the same time, the other main surface of the lead frame 20 may be subjected to a roughening treatment by etching or the sand blast plating method. Further, when a lead frame is used in which the IC chip 16 is attached to the electrode terminals 12 without a die pad 11, the die pad resin with which the IC chip is mounted may be insulating.

Effect of the Invention

Because the semiconductor integrated circuit device of this invention is formed by establishing one or more stair or stepped components on the tip surface of the lead frame board and with sealing resin in a configuration that covers these stepped components, the electrode terminals are not readily peeled off in the presence of external force. Because the electrode terminals are not peeled off even in the face of thermal strain such as during thermal impact tests, a product of high reliability can be obtained.

4. Brief Explanation of the Figures

Figure 1 is an enlarged oblique view of an example of the semiconductor integrated circuit device of this invention, Figures 2a and b are an upper surface view and a cross-sectional view that show the structure of the lead frame that is used in this invention, Figures 3a through c are cross-sectional views that show the manufacturing steps of the semiconductor integrated circuit of this invention and Figure 4 is a cross-sectional view that shows the structure of a semiconductor integrated circuit device in which a conventional lead frame is used.

12 – electrode terminal; 13 – one main surface; 14- the other main surface; 15 – stair component; 16 – IC chip; 17 – wire; 18 – sealing resin; 19 – reinforcing bar; 20 – lead frame.

Name of Agent: Toshio Nakao, Patent Attorney, And 1 Other

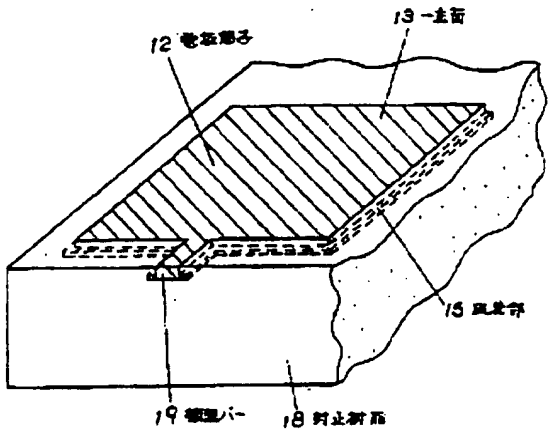

Figure 1

12 – electrode terminal

13 – one main surface

15 – stair component

18 – sealing resin

19 – reinforcing bar

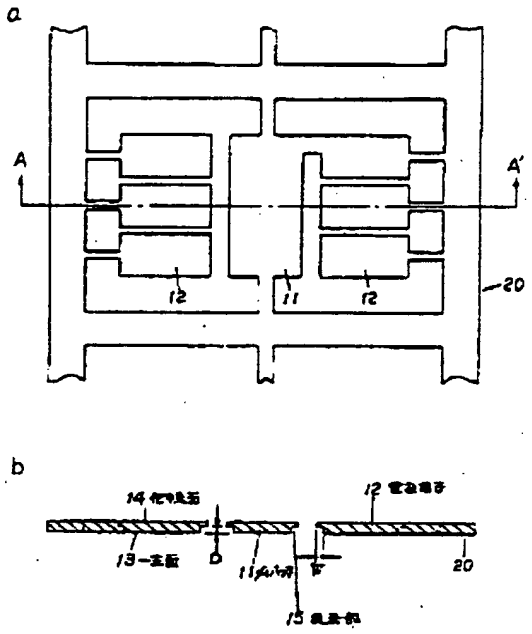

Figure 2

a [top figure]

b [bottom figure]

11 – die pad

12 - electrode terminal

13 – one main surface

14 – other main surface

15 – stair component

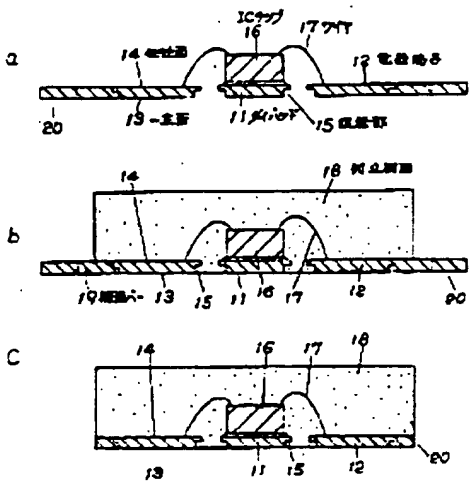

Figure 3

a

11 – die pad

12 – electrode terminal

13 – one main surface

14 – other main surface

15 – stair component

16 – IC chip

17 - wire

b

18 – sealing resin

19 – reinforcing bar

Figure 4